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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,903	11/29/2000	Pooi See Lee	CHAR.P0003	3317

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EXAMINER
GARCIA, JOANNIE A

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,903	LEE ET AL.	
	Examin r	Art Unit	
	Joannie A Garcia	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The disclosure is objected to because of the following informalities: On page 4, line 7, "poorly activated" should be replaced with --poorly activated.--. The period at the end of the sentence after "activated" is missing.

Appropriate correction is required.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, lines 5-6, it is unclear what is recited through the use of "at least one of n-type doping and p-type doping a portion of said silicon substrate to form said source/drain structures".

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-6, 8, and 11, are rejected under 35 U.S.C. 102(a) as being anticipated by Wu (U.S. Patent 6,090,653).

Wu discloses forming a processed substrate including partially fabricated integrated circuit components and a silicon substrate 2 (Figure 4), wherein said processed substrate comprises forming dielectric regions 4 in said silicon substrate that electrically isolate

neighboring integrated circuit devices (Figure 1, and Column 3, lines 56-62), forming source/drain regions 12 in said silicon substrate (Figure 3, and Column 4, lines 22-30), depositing a gate dielectric material 6 and a polycrystalline silicon gate material 8 onto said silicon substrate and selectively etching (Figure 2, and Column 4, lines 1-5, and 13-14), depositing a dielectric material onto said silicon substrate and selectively etching to form dielectric spacers 14 (Figure 4, and Column 4, lines 31-35), incorporating nitrogen into said processed substrate (Figure 5), by doping with nitrogen (Column 4, lines 36-38) and by implanting nitrogen ions into said processed substrate comprising a blanket N_2^+ ion implantation of said processed substrate (Column 4, lines 36-38), depositing nickel onto said processed substrate (Figure 6, and Column 4, lines 61-64), and annealing said processed substrate so as to form nickel-monosilicide 18/20 (Figure 7, Column 4, lines 65-67, and Column 5, lines 3-5), wherein said annealing said processed substrate so as to form nickel-monosilicide comprises one-step thermal processing at 700 °C (Column 4, lines 65-67, and Column 5, lines 1-2). Wu also teaches annealing said processed substrate prior to depositing nickel (Column 4, lines 5-9).

Claims 7, 9, and 12-14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu as applied to claims 1-6, 8, and 11 above, and further in view of Ohguro (U.S. Patent 5,840,626), in combination with the following comments.

Wu teaches removing unreacted nickel after said processed substrate so as to form nickel mono-silicide (Column 5, lines 2-3). Wu does not teach that said annealing said processed substrate prior to said depositing nickel comprises rapid thermal processing at a temperature between 800 °C and 1000 °C for a duration of between 30 seconds and 60 seconds; performing a

series of integrated circuit fabrication procedures after said removing unreacted nickel, including depositing a dielectric material onto said processed substrate and selectively etching, planarazing said processed substrate, and depositing metal onto said processed substrate and selectively etching to form metal lines; and, removing unreacted nickel using a solution containing at least sulfuric acid and hydrogen peroxide. Wu does not teach either that said annealing said processed substrate so as to form nickel mono-silicide and said removing unreacted nickel comprise a process to form a gate electrode including nickel mono-silicide and polycrystalline silicon that is electrically isolated from a source/drain contact including nickel mono-silicide and single crystal silicon.

Ohguro discloses forming a processed substrate including partially fabricated integrated circuit components and a silicon substrate 31 (Figure 18B), wherein said processed substrate comprises forming dielectric regions 32 in said silicon substrate that electrically isolate neighboring integrated circuit devices (Figure 18A, Column 8, lines 42-44), forming source/drain regions 36/37 in said silicon substrate (Figure 18B, and Column 8, lines 49-53, and 59-60), depositing a gate dielectric material 34 and a polycrystalline silicon gate material 33 onto said silicon substrate and selectively etching (Figure 18B, and Column 8, lines 45-48), depositing a dielectric material onto said silicon substrate and selectively etching to form dielectric spacers 35 (Figure 18B, and Column 8, lines 53-58), depositing nickel 39 onto said processed substrate (Figure 18C, Column 8, line 67, and Column 9, line 1), incorporating nitrogen into said processed substrate (Column 9, lines 2-4), and annealing said processed substrate so as to form nickel-monosilicide 41 (Figure 18D, and Column 9, lines 7-11). Ohguro discloses as well, removing unreacted nickel after said processed substrate so as to form nickel mono-silicide

(Figure 18E, and Column 9, lines 14-17), performing a series of integrated circuit fabrication procedures after said removing unreacted nickel, including depositing a dielectric material 42 onto said processed substrate and selectively etching (Figure 18F), planarazing said processed substrate (Figure 18F), and depositing metal onto said processed substrate and selectively etching to form metal lines 43 (Figure 18F), and removing unreacted nickel using a solution containing at least sulfuric acid and hydrogen peroxide (Column 9, lines 14-17). Ohguro also teaches that said annealing said processed substrate so as to form nickel mono-silicide and said removing unreacted nickel comprise a process to form a gate electrode including nickel mono-silicide and polycrystalline silicon that is electrically isolated from a source/drain contact including nickel mono-silicide and single crystal silicon (Figure 18F). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wu and Ohguro to enable the necessary contact formation step to be performed in Wu, and to obtain a semiconductor device having a flat boundary at a silicon substrate (Ohguro, Column 2, lines 12-13).

Ohguro discloses as well, annealing said processed substrate prior to said depositing nickel, wherein said annealing said processed substrate prior to said depositing nickel comprises rapid thermal processing at a temperature of 1000 °C. It would have been a matter of routine optimization within the teachings of Ohguro to determine a suitable duration of time to achieve the rapid thermal processing step. It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wu and Ohguro to enable the annealing step of Wu prior to deposition of nickel 16 to be performed, and to obtain a semiconductor device having a flat boundary at a silicon substrate (Ohguro, Column 2, lines 12-13).

With respect to claim 7, it would have been a matter of routine optimization within the teachings of Wu to determine a suitable dosage and energy to achieve the blanket N_2^+ ion implantation step.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu as applied to claims above, and further in view of O'Brien, and the following comments.

Wu discloses forming said nickel by sputter deposition (Column 4, lines 61-64). Wu does not teach that said depositing nickel comprises applying a solution including hydrogen fluoride to said processed substrate, and that said sputter deposited nickel is between 100 angstroms and 300 angstroms. O'Brien teaches sputter depositing nickel applying a solution including hydrogen fluoride (Column 2, lines 10-13). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wu and Ohguro to enable the depositing step of nickel 16 of Wu, and to obtain simplicity of the removal of metal/nitride plus silicide filaments with selectivity and control for the nickel silicide (O'Brien, Column 1, lines 65-67). It would have been a matter of routine optimization within the teachings of Wu to determine a suitable depth to achieve nickel deposition step.

Claim 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: the prior art taken alone or in combination neither discloses nor makes obvious the instant invention including formation of a processed substrate including partially fabricated integrated circuit components and a silicon substrate, incorporating nitrogen into said processed substrate, depositing nickel onto said processed substrate, annealing said processed substrate so as to form nickel-monosilicide, and applying said incorporated nitrogen and said depositing nickel to a region smaller than the entire top surface of the processed substrate. Therefore, the prior art of record neither anticipates nor renders obvious the claimed subject matter.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. **See MPEP 203.08**.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner J. Garcia whose telephone number is (703) 308-2544. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax number for this group is

(703) 308-7722 (and 7724), and (703) 305-3431 (and 3432). MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

JAG
9/30/02

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800